REMARKS

The present application was filed on September 30, 2003 with claims 1-20. Claims 1-5 and 7-20 are pending in the application. Claims 1, 19 and 20 are the pending independent claims.

Claims 1-5 and 7-20 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,764,641 (hereinafter "Lin").

In this response, Applicant traverses the §102(b) rejection. Applicant respectfully requests reconsideration of the present application in view of the remarks below.

With regard to the §102(b) rejection, Applicant initially notes that MPEP §2131 specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). For the reasons identified below, Applicant submits that the Examiner has failed to establish anticipation of claims 1-5 and 7-20 by Lin.

Independent claim 1 is directed to a processor that comprises a plurality of input ports, memory circuitry for storing data blocks associated with protocol data units and received by the processor at the input ports, and controller circuitry coupled to the memory circuitry and operative to discard certain ones of the data blocks received at the input ports in an oversubscription condition in which the received data blocks exceed a designated capacity of the processor. A discarded data block indicator is generated for a given one of the input ports if a data block received at the given input port for a particular protocol data unit is discarded, and one or more additional data blocks received at the given input port for the particular protocol data unit are discarded based at least in part on the discarded data block indicator. Moreover, the controller circuitry is operative to maintain separate discarded data block indicators for respective ones of the plurality of input ports.

Thus, in the invention as set forth in claim 1, each of the plurality of input ports has its own separate discarded data block indicator.

In an illustrative embodiment of the invention, described in the specification at page 10, lines 5-11, the controller 204 in network processor 102 as shown in FIG. 2 maintains separate state bits for each of the N input ports 200-1 through 200-N in the set of input ports 200. See steps 304 through 308 of the flow diagram in FIG. 3. As indicated at page 7, lines 11-13, such an approach advantageously reduces the number of PDUs that are corrupted via discarded data blocks in an oversubscription condition, thereby improving processor throughput and performance. It is to be appreciated, of course, that these particular aspects of the illustrative embodiment are presented by way of example only, and are not to be construed as limitations of the claimed invention.

The Examiner in formulating the §102(b) rejection of claim 1 argues that each and every one of the above-noted limitations is met by Lin. Applicant respectfully disagrees. For example, in characterizing the Lin reference as allegedly meeting the limitation of independent claim 1 regarding controller circuitry operative to maintain separate discarded data block indicators for respective ones of the plurality of input ports, the Examiner relies primarily on column 6, lines 55-61, and FIG. 3B, steps 111-112, of Lin. See the final Office Action, at page 4, lines 1-3. However, Applicant respectfully submits that the relied-upon portions of Lin fail to anticipate the limitation at issue. The Lin reference, in column 6, lines 55-61, states the following, with emphasis supplied:

> If the queue length exceeds the EPD buffer threshold, the controller 18 discards the cell, since the controller cannot ensure that it will have available sufficient buffer space to hold the remaining cells of the packet as they arrive. The controller thus pre-empts what is expected to be a fragmented packet. The controller then sets an EPD flag that is associated with the virtual circuit identified in the cell (steps 111-112).

The Examiner apparently argues that the early packet discard (EPD) flag of Lin is anticipatory of the recited discarded data block indicator. However, claim 1 clearly indicates that separate such discarded data block indicators are maintained for respective input ports of the processor. The relied-upon portions of Lin indicate that EPD flags are set for particular virtual circuits that are identified in a corresponding cell. Thus, the EPD flags are not maintained for respective input ports of the processor.

It is therefore believed that the teachings of Lin fail to meet each and every limitation of independent claim 1. In fact, the relied-upon portion of Lin not only fails to teach or suggest the maintenance of separate discarded data block indicators for respective input ports, but appears to actively teach away from such an arrangement by setting EPD flags for particular virtual circuits. Furthermore, the EPD flags of Lin fail to provide the advantages associated with the embodiment of the invention described above.

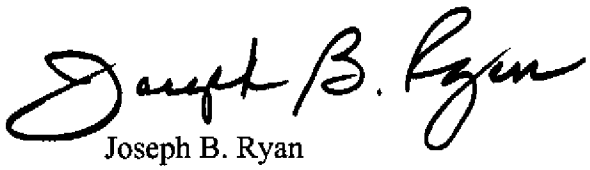
Independent claims 19 and 20 include limitations similar to those of claim 1, and are therefore believed allowable for reasons similar to those described above with reference to claim 1.

Dependent claims 2-5 and 7-18 are believed allowable for at least the reasons identified above with regard to claim 1.

In view of the foregoing, claims 1-5 and 7-20 are believed to be in condition for allowance.

As indicated previously, a Notice of Appeal is filed concurrently herewith.

Respectfully submitted,



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Enclosure(s): Notice of Appeal